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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/938,643	08/27/2001	Hajime Akimoto	A8319.0002	2809

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EXAMINER
SHAPIRO, LEONID

ART UNIT	PAPER NUMBER
2673	6

DATE MAILED: 09/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/938,643	AKIMOTO ET AL.	
	Examiner	Art Unit	
	Leonid Shapiro	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-4,6,8-14,20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima et al. (US Patent No. 6,181,314 B1) in view of Negishi et al. (US Patent No. 5,528,241) and further in view of Yamagata et al. (Pub. No.: US 2001/0028336 A1).

As to claim 1, Nakajima et al. teaches an image display apparatus having a display unit for displaying an image (See Fig. 1, item 1020, in description See Col. 3, Lines 7-14) and a drive unit for driving this display unit, the drive unit being connected by a plurality of signal lines (See Fig. 1, item 1040), wherein display unit comprises a plurality of display pixels arranged in a matrix form (See Fig. 1, item 1010, in description See Col. 3, Lines 7-14).

Nakajima et al. does not show impedance converters connected to an output of the ladder resistor.

Negishi et al. in his video signal processor teaches ladder resistor portion and impedance converter (amplifier in the Negishi et al. reference should be considered as impedance converter, because it has high input impedance and low output impedance to prevent loading the resistor ladder) (See Fig. 2, items 20-21, in description See from Col. 2, Line 64 to Col. 3, Line15). (Both Nakajima et al. and Negishi et al. are in analogues art of video signal processing). It would have been obvious to one of ordinary skill in the art at the time of invention use the ladder resistor and impedance converter as shown by Negishi et al. in Nakajima et al apparatus as part

of D-A converter to provide an improved output circuit (See Fig. 2, item 15, in description See Col. 1, Lines 66-67 in Nakajima et al. reference).

Nakajima et al. and Negishi et al. do not show gray level voltage wires constituting output line connected to the impedance converters, and a gray level voltage selector connected to the gray level voltage wires.

Yamagata et al. teaches gray level voltage wires constituting output line, and a gray level voltage selector connected to the gray level voltage wires (See Fig. 2, item 3, NLN, in description See page 4, paragraph 0063). It would have been obvious to one of ordinary skill in the art at the time of invention use a gray level voltage selector as shown by Yamagata et al. in Nakajima et al and Negishi et al. apparatus as part of D-A converter to provide an improved output circuit (See Fig. 2, item 15, in description See Col. 1, Lines 66-67 in Nakajima et al. reference).

As to claim 20, Nakajima et al. teaches an image display terminal system, comprising a plurality of display pixels arranged in a matrix form to display an image (See Fig. 1, item 1010, in description See Col. 3, Lines 7-14); a group of signal lines provided for each column to transmit analog image signals and connected to display pixels (See Fig. 1, item 1020, in description See Col. 3, Lines 7-14) a drive circuit for driving the display pixels and the group of signal lines at prescribed timing, and means for causing the display pixels to display an image in a prescribed sequence on the basis of inputted image display data (See Figs. 1-2, item 1040, 11-18, C1-Cn, in description See Col. 3, lines 7-44).

Nakajima et al. does not show a ladder resistor, impedance converters connected to an output of the ladder resistor.

Negishi et al. teaches ladder resistor portion and amplifier (See Fig. 2, items 20-21, in description See from Col. 2, Line 64 to Col. 3, Line15). It would have been obvious to one of ordinary skill in the art at the time of invention use the ladder resistor and impedance converter as shown by Negishi et al. in Nakajima et al apparatus as part of D-A converter to provide an improved output circuit (See Fig. 2, item 15, in description See Col. 1, Lines 66-67 in Nakajima et al. reference).

Nakajima et al. and Negishi et al. do not show group of signal lines are connected to the gray level voltage wires via a gray level voltage selector, each gray level voltage wire is connected to the output of the ladder resistor via impedance converters.

Yamagata et al. teaches gray level voltage wires constituting output line, and a gray level voltage selector connected to the gray level voltage wires (See Fig. 2, item 3, NLN, in description See page 4, paragraph 0063). It would have been obvious to one of ordinary skill in the art at the time of invention use a gray level voltage selector as shown by Yamagata et al. in Nakajima et al and Negishi et al. apparatus as part of D-A converter to provide an improved output circuit (See Fig. 2, item 15, in description See Col. 1, Lines 66-67 in Nakajima et al. reference).

Nakajima et al, Negishi et al. and Yamagata et al. do not show the gray level voltage selector and the gray level voltage wires are provided over a single substrate.

Since in Nakajima et al, all TFT switches configured by polycrystalline Si, it would have been obvious if not inherent to one of ordinary skill in the art at the time of invention to place the gray level voltage selector and the gray level voltage wires on the same substrate in Nakajima et al, Negishi et al. and Yamagata et al. apparatus.

As to claims 2-3, Nakajima et al. teaches gray level voltage selector as part of D-A converter (See Fig. 2, item 15) connected to plurality of signal lines (See Figs. 1-2, items 15, 17-18, C1-Cn, in description See Col. 3, Lines 14-44).

As to claim 4, Nakajima et al. teaches impedance converters are configured by drain-grounded field-effect transistors as the output buffers. (See Fig. 3, items 21-22, in description See Col. 3, Lines 45-46.

Nakajima et al. does not teach impedance converters (amplifiers inside of the DAC between resistor ladder and a gray level voltage selector. It would have been obvious to one of ordinary skill in the art at the time of invention use a impedance converters are configured by drain-grounded field-effect transistors in Nakajima et al, Negishi et al. and Yamagata et al. apparatus as part of D-A converter instead of the output buffers (See Fig. 2, item 15).

As to claim 6, Nakajima et al. teaches offset canceling unit for detecting and eliminating any offset voltage between input and output (See Fig. 3, items 23-27, in description See from Col. 3, Line 44 to Col. 4, Line 58).

As to claim 8, Nakajima et al. teaches liquid crystal display device.

Nakajima et al. does not show liquid crystal in region between the pixel electrode and the counter electrode. It would have been obvious if not inherent to one of ordinary skill in the art at the time of invention to use LC material in Nakajima et al, Negishi et al. and Yamagata et al. in region between the pixel electrode and the counter electrode.

As to claim 9, Yamagata et al. teaches a gray level voltage selector is configured by an analog switch using a field effect transistor (See Fig. 2, item Tr, in description See page 4, paragraph 0063).

As to claim 10-12, Nakajima et al, Negishi et al. and Yamagata et al. do not show ladder resistor, voltage selector and impedance converters are configured by a polycrystalline Si and on the same substrate.

Since in Nakajima et al, all TFT switches configured on the same substrate, it would have been obvious if not inherent to one of ordinary skill in the art at the time of invention to configure the ladder resistor, voltage selector and impedance converters using polycrystalline Si film on the same substrate in Nakajima et al, Negishi et al. and Yamagata et al. apparatus.

As to claim 13, Negishi et al. teaches ladder resistor is configured as one resistor (See Fig. 2, item20, in description See from Col. 2, Line 64 to Col. 3, Line 32 and Abstract).

As to claim 14, Yamagata et al. teaches ladder resistor is a pair of resistors group, one each for positive voltage gray level generation and inverted polarity gray level generation (See Fig. 2, item 6, in description See page 4, paragraph 0063).

2. Claims 5, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima et al, Negishi et al. and Yamagata et al. in view of Morita (US Patent No. 6,366,065 B1).

As to claim 5, Nakajima et al, Negishi et al. and Yamagata et al. do not show impedance converters configured by differential amplifying circuit using field-effect transistors.

Morita teaches impedance converters configured by differential amplifying circuit using field-effect transistors (See Fig. 10, 12, items 72, QP, in description See Col. 10, Lines 1-9). It would have been obvious to one of ordinary skill in the art at the time of invention use a differential amplifying circuit using field-effect transistors as shown by Morita in Nakajima et

al., Negishi et al. and Yamagata et al. apparatus as part of D-A converter instead of the output buffers (See Fig. 2, item 15).

As to claim 7, Nakajima et al, Negishi et al. and Yamagata et al. do not show means for suspending the functioning of the impedance converters and circuits for short-circuiting the input and output terminals of the impedance converters.

Morita teaches means for suspending the functioning of the impedance converters and circuits for short-circuiting the input and output terminals of the impedance converters (See Fig. 5, items 72, Q2, in description See Col. 6, Lines 39-59). It would have been obvious to one of ordinary skill in the art at the time of invention use a differential amplifying circuit using field-effect transistors as shown by Morita in Nakajima et al., Negishi et al. and Yamagata et al. apparatus as part of D-A converter instead of the output buffers (See Fig. 2, item 15).

3. Claims 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima et al , Negishi et al. and Yamagata et al. in view of Kane (US Patent No. 6,229,508 B1).

As to claims 16, 19, Nakajima et al. teaches a driving method for an image display apparatus having a plurality of display pixels arranged in a matrix form to display an image (See Fig. 1, item 1010, in description See Col. 3, Lines 7-14), a group of signal lines provided for each column to transmit analog image signals and connected to display pixels (See Fig. 1, item 1020, in description See Col. 3, Lines 7-14) and a drive circuit for driving the display pixels and the group of signal lines at prescribed timing, and writing the analog image signal voltages into the pixel capacitances of the display pixels to display the image (See Figs. 1-2, item 1040, 11-18, C1-Cn, in description See Col. 3, lines 7-44).

Nakajima et al. does not show a ladder resistor.

Negishi et al. teaches ladder resistor portion and amplifier (See Fig. 2, items 20-21, in description See from Col. 2, Line 64 to Col. 3, Line15). It would have been obvious to one of ordinary skill in the art at the time of invention use the ladder resistor and impedance converter as shown by Negishi et al. in Nakajima et al apparatus as part of D-A converter (See Fig. 2, item 15).

Nakajima et al. and Negishi et al. do not show gray level voltage wires constituting output line from impedance converters, and a gray level voltage selector connected to the gray level voltage wires.

Yamagata et al. teaches gray level voltage wires constituting output line, and a gray level voltage selector connected to the gray level voltage wires (See Fig. 2, item 3, NLN, in description See page 4, paragraph 0063). It would have been obvious to one of ordinary skill in the art at the time of invention use a gray level voltage selector as shown by Yamagata et al. in Nakajima et al and Negishi et al. apparatus as part of D-A converter (See Fig. 2, item 15).

Nakajima et al. teaches display driving method for displaying an image by writing analog image signal voltages via signal lines into pixel capacitances of individual pixels in a display unit, wherein the analog image signal voltages are written in two separate phases when the analog image signal voltages are to be written onto the signal line (See Figs. 3-4, items 21-26,T1,T2, in description See from Col. 3, Line 45 to Col. 5, Line 7).

Nakajima et al., Negishi et al and Yamagata et al. do no show the third phase.

Kane teaches three separate phases when the analog image signal voltages are to be written onto the signal line (See Figs. 5-6, items 550,530,510, PRECHRGE,

AUTOZERO,WRITE DATA, in description See from Col. 5, Line 43 to Col. 6, Line 50). It would have been obvious to one of ordinary skill in the art at the time of invention to use the driver as shown by Kane in Nakajima et al., Negishi et al and Yamagata et al. apparatus to provide an improved output circuit in display device where a power consumption is low and output potential variations are minimized (See from Col. 1, Line 65 to Col. 2,Line2 in Nakajima et al. reference).

As to claim 15, Nakajima et al, Negishi et al. and Yamagata et al. do not show a luminescent type of display pixels controlled by entered analog image signal and having a light emitting function for displaying an image with luminescence generated by a current flowing between a positive and a negative electrode.

Kane teaches a luminescent type of display pixels controlled by entered analog image signal and having a light emitting function for displaying an image with luminescence generated by a current flowing between a positive and a negative electrode (See Figs. 1-3, item 304, in description See Col. 3, Lines 28-62). It would have been obvious to one of ordinary skill in the art at the time of invention to use the driver as shown by Kane in Nakajima et al., Negishi et al. and Yamagata et al. apparatus to incorporate a LED (OLED) pixel structure (See Col.2, Lines 9-12 in the Kane reference).

As to claim 17, Nakajima et al. teaches display driving method for displaying an image by writing analog image signal voltages via signal lines into pixel capacitances of individual pixels in a display unit, wherein the analog image signal voltages are written in two separate phases when the analog image signal voltages are to be written onto the signal line (See Figs. 3-4, items 21-26,T1,T2, in description See from Col. 3, Line 45 to Col. 5, Line 7).

Nakajima et al , Negishi et al. and Yamagata et al. do not show the third phase.

Kane teaches three separate phases when the analog image signal voltages are to be written onto the signal line (See Figs. 5-6, items 550,530,510, PRECHRGE, AUTOZERO,WRITE DATA, in description See from Col. 5, Line 43 to Col. 6, Line 50). It would have been obvious to one of ordinary skill in the art at the time of invention to use the driver as shown by Kane in Nakajima et al , Negishi et al. and Yamagata et al. apparatus to provide an improved output circuit in display device where a power consumption is low and output potential variations are minimized (See from Col. 1, Line 65 to Col. 2,Line2 in Nakajima et al. reference).

As to claim 18, Kane teaches signal lines are provided with voltage resetting circuits, and analog image signal voltages are written in three separate phases after the voltages of the signal lines are reset in advance by the resetting circuits (See Figs. 5-6, items 550,530,510, PRECHRGE, AUTOZERO,WRITE DATA, in description See Col. 6, Lines 15 and 36).

Response to Amendment

4. Applicant's arguments filed on 08-21-03 have been fully considered but they are not persuasive.

On page 9, 1st, 3rd and 4th paragraphs of the Remarks Applicants stated, that Nakajima, Negishi and Yamagata et al. fail to disclose all of the limitations of claim 1, like "impedance converters connected to an output of a ladder resistor, gray level voltage wires constituting output lines connected to the impedance converters...". The same in 3rd paragraph regarding Negishi and Yamagata et al. references. The same in 4th paragraph, in relation to connection

between data latch and gates of each transistor Tr. However, Applicant's could not show non-obviousness by attacking references individually where, as here the rejections are based on combination of references. In re Keller, 208 USPQ 871 (CCPA 1981).

On the same page, 2nd paragraph of the Remarks Applicants stated, that Nakajima differs from Applicant's invention since the number of impedance converters need not to be as many as number of signal lines as in Nakajima. However, claim 1 does not have above mentioned limitation. The same related to the transferring phases.

On page 10, 3rd paragraph of the Remarks regarding claims 16-20, Applicants stated, that Kane do not disclose "a plurality of gray level voltage wires connected to an output of the ladder resistor" and the other limitations. However, Applicant's could not show non-obviousness by attacking references individually where, as here the rejections are based on combination of references. In re Keller, 208 USPQ 871 (CCPA 1981).

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 703-305-5661. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-305-4938. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4750.

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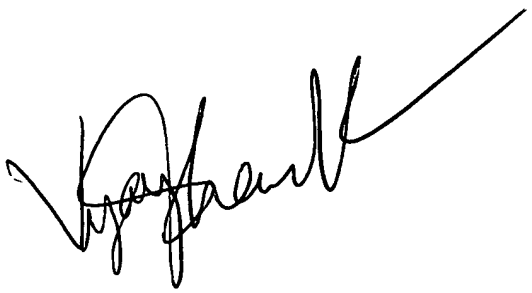

VIJAY SHANKAR
PRIMARY EXAMINER